Effects of Parasitics on An Active Clamp Assisted Phase Shifted Full Bridge Converter Operation

Manmohan Mahapatra, Anirban Pal and Kaushik Basu
Department of Electrical Engineering,
Indian Institute of Science, Bangalore
Bangalore-560012, India
{manmohanm, anirbanp, kbasu}@iisc.ac.in

2021 IEEE Energy Conversion Congress and Exposition (ECCE) | 978-1-7281-5135-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECCE47101.2021.9596057

***Abstract*—The phase-shifted full bridge (PSFB) converter is widely used for isolated DC-DC applications due to simple control and zero voltage switching (ZVS) capability. The ZVS is achieved with the help of primary bridge device capacitances and transformer leakage inductance. The secondary diode parasitic capacitances cause high voltage stress and affect the converter voltage gain. In literature, several snubber circuits are presented to clamp the voltage overshoot, but the change in voltage gain due to secondary diode capacitances is ignored. In this paper the operation of PSFB with an active clamp is analysed considering all circuit parasitics including transformer leakage inductance, primary device and secondary diode capacitances. A closed form expression of the voltage gain is analytically derived. It is observed that the voltage gain is independent of snubber clamp voltage. Other than the known duty cycle loss due to leakage inductance, the output voltage has a duty cycle gain due to secondary diode capacitance. The paper also presents an estimation technique of key parasitics through experiment. These findings are essential for the design of a PSFB particularly for high-step-up application. A prototype of 1.5kW with input 400V and output 1.25kV is built and tested. Key experimental results are shown to verify the presented analysis of PSFB considering all parasitics.**

***Index Terms*—Phase-shifted full bridge, parasitics, leakage inductance, device output capacitance, active clamp, ZVS.**

I. Introduction

The phase shifted full bridge (PSFB) converter is widely popular for medium power isolated DC-DC applications [1]–[8]. Active and zero are the two operational states of PSFB [9]. In the active state, power is transferred from input to output port whereas power free-wheels in zero state. The PSFB has some attractive features like- simple duty-cycle control, zero voltage switched primary bridge without additional snubber and linear relationship of the steady-state voltage gain with duty ratio. Ideally for a given dc bus, the gain is independent of load and can be controlled linearly by varying duty-ratio. The transformer leakage inductance and device capacitances help to achieve ZVS of the converter.

But the PSFB has few major limitations. The ZVS depends on load current. Secondary diodes experience high voltage stress at the end of zero to active state transition due to parasitic resonance. In literature, several active [10], [11] and passive [12], [13] snubber circuits are given to limit the voltage stress. Additionally in zero to active state transition due to transformer leakage inductance, the rectifier output voltage remains zero during the diode bridge current commutation. This results in significant duty cycle loss. These effects of the parasitics were analysed in details in the existing PSFB literature [9], [10]. The zero voltage (ZVS) transitions considering primary device capacitances and transformer leakage inductance were investigated.

In the existing analysis, the effects of secondary diode capacitances are either ignored or only considered to explain the secondary voltage overshoot phenomena [9], [12]. It is observed that the PSFB voltage gain is affected by the secondary diode capacitances. Additionally, due to the secondary diode capacitances the primary current falls significantly during active to zero state transition which otherwise is assumed to remain constant in ideal operation. The reduced current in zero state further affects soft-switching. The above effects are dominant in a step-up PSFB due to large leakage inductance and large reflected diode capacitances. Hence the existing analysis is incomplete and the PSFB operation with all dominant parasitics needs to be explored.

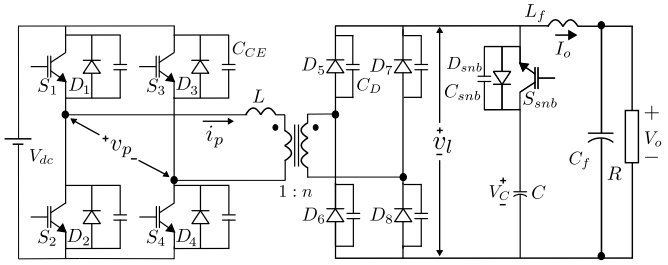


Fig. 1. PSFB converter with circuit parasitics and active snubber.

This paper presents a detailed circuit analysis of PSFB operation considering all dominant parasitics including transformer leakage inductance, primary device and secondary diode capacitances. A commonly used active snubber [10] is employed at the secondary. The major contributions and key observations are as follows. (i) A closed form expression of average output voltage is derived. (ii) Other than the well-known duty cycle loss in the average output voltage due to transformer leakage inductance, a duty cycle gain due to secondary parasitic capacitances is observed. (iii) The average output voltage is independent of the active clamp voltage. (iv) An analytical expression of primary current in zero state is provided. This helps to properly select the dead-time for soft-

switching. (v) The paper also presents an estimation technique of key parasitics through experiment. The mode by mode converter operation is verified experimentally with a 1.5kW, 400V-1.25kV PSFB prototype. The expressions derived in this paper helps in optimally design the converter.

The paper is organised as follows. The converter operation considering parasitics is presented in Section II. In Section III an analytical closed form expression of the output voltage is given. Estimation methods of the converter parasitics are discussed in section IV. Key experimental results are presented in section V to verify the converter operation.

II. Circuit Operation and DC Analysis

In Fig. 1, a PSFB converter is shown. Fig. 2a presents the ideal waveforms of the converter (without considering any parasitic). v_p and i_p are transformer primary voltage and current respectively. v_l is the diode bridge output voltage. An active clamp circuit with clamp voltage V_C is employed after the diode bridge. The snubber capacitor is large enough so that it can be modelled as a voltage source V_C. The snubber device (S_{snb}) is switched at low frequency to maintain charge balance of the snubber capacitor. In a normal switching cycle S_{snb} is kept OFF. The design of the snubber is given in [14]. The parasitics considered in the analysis are given as follows- primary device capacitance (C_{CE}), secondary diode capacitance (C_D), transformer leakage inductance referred to primary (L) and snubber device parasitic capacitance (C_{snb}). The snubber branch has effective capacitance C_{snb} as the snubber capacitance is relatively large. Over a transformer flux balance cycle (T_s), the PSFB has two active and two zero states. The converter operation is symmetrical over $T_s/2$ and has 9 modes. The primary switches have gating signals ($G_1 - G_4$) with period T_s and 50% duty ratio. Key waveforms over $T_s/2$ are shown in Fig. 2b. The output filter inductor current is modelled as a constant sink, I_o with negligible ripple.

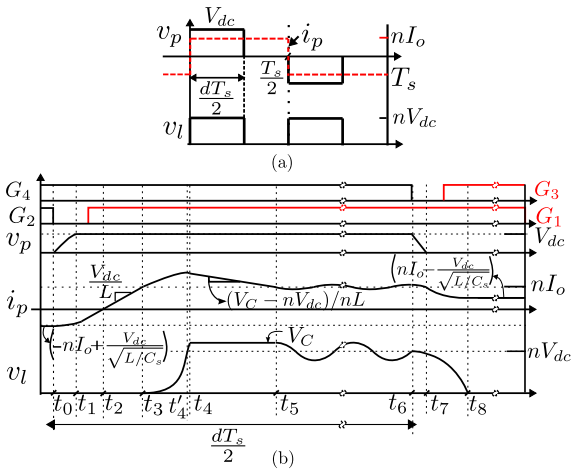


Fig. 2. Waveforms- (a) considering ideal operation of PSFB, (b) considering circuit parasitics

The converter is in zero state when $t < t_0$ (Fig. 2b) as S_2 and D_4 are in conduction, shorting the transformer primary terminals ($v_p = 0$). In secondary all four diodes are conducting. The primary current is given as $i_p(t) \approx -\left(nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}\right)$ and is derived in Mode 8. where $C_S = n^2(2C_D + C_{snb})$ and n is the transformer secondary to primary turns ratio.

A. Mode 1: $t_0 < t < t_1$

This mode starts when S_2 is turned off at $t = t_0$. Due to presence of switch capacitance C_{CE}, voltage across the device cannot change immediately. Channel current through the device falls first and then the device drain to source voltage starts rising. So, turn OFF of S_2 is a zero voltage switching (ZVS) transition. As the magnitude of i_p is lower than load current nI_o (see Fig. 2b), all four diodes of the secondary rectifier are in conduction, shorting the transformer secondary. The equivalent circuit during this mode is shown in Fig. 3a. $C_P = 2C_{CE}$ is the effective primary side capacitance. Solving

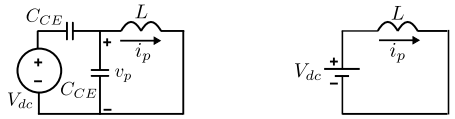


Fig. 3. Equivalent Circuits in (a) Mode 1, (b) Mode 2

the L-C dynamics with initial conditions- $i_p(t_0) \approx -nI_o + \frac{V_{dc}}{\sqrt{L/C_S}}$ and $v_p(t_0) = 0$, i_p and v_p are given in (1).

$$
\begin{aligned}
i_p(t) &\approx \left(-nI_o + \frac{V_{dc}}{\sqrt{L/C_S}}\right)\cos\left(\omega_1(t-t_0)\right) \\
v_p(t) &\approx \left(nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}\right)\sqrt{\frac{L}{C_P}}\sin\left(\omega_1(t-t_0)\right) \\
t_I &= (t_1 - t_0) = \sqrt{LC_P}\sin^{-1}\left(\frac{\frac{V_{dc}}{\sqrt{L/C_P}}}{nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}}\right)
\end{aligned}
\tag{1}
$$

where $\omega_1 = \frac{1}{\sqrt{LC_P}}$. The device voltages are given as $v_{S_1} = (V_{dc} - v_p)$ and $v_{S_2} = v_p$. This mode ends at t_1 when v_p reaches V_{dc} and anti-parallel diode of S_1 is forward biased. The time interval for Mode 1 (t_I) is given in (1). This mode will end if $\frac{V_{dc}}{\sqrt{\frac{L}{C_P}}\left(nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}\right)} < 1$ (using (1)). The above condition can further be simplified as $\frac{V_{dc}}{nI_o}\frac{\sqrt{C_P}+\sqrt{C_S}}{\sqrt{L}} < 1$. In case of a step-up PSFB with large L, typically at rated load, $\frac{V_{dc}}{nI_o}\frac{\sqrt{C_P}+\sqrt{C_S}}{\sqrt{L}} << 1$. And hence following approximations are made. $t_I \approx \frac{V_{dc}C_P}{nI_o}$ and $i_p(t_1) \approx -nI_o + \frac{V_{dc}}{\sqrt{L/C_S}}$. Meaning, i_p remains almost same, leading to a linear change in the capacitor voltage (v_p).

B. Mode 2: $t_1 < t < t_2$

In this mode the anti-parallel diodes of S_1 and S_4 (D_1 and D_4) are in conduction. As the applied voltage v_p is against the direction of i_p, it falls linearly. Equivalent circuit during

this mode is shown in Figure 3b. The primary current is given as in (2).

$$i_p(t) \approx -nI_o + \frac{V_{dc}}{\sqrt{L/C_S}} + \frac{V_{dc}}{L}(t - t_1) \tag{2}$$

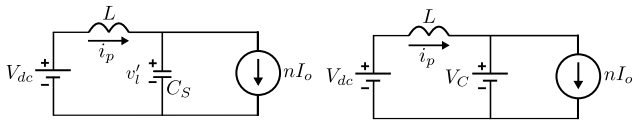
To ensure ZVS turn ON, the gating pulse of S_1 is applied in this mode when the anti-parallel diode is in conduction. At the end of this mode i_p becomes zero and changes the direction. The interval of this mode can be estimated solving (2) and is given as $t_{II} = t_2 - t_1 \approx \left(nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}\right)\frac{L}{V_{dc}}$. The ZVS turn ON of $S_1 - S_2$ can be ensured when the dead time (DT) is $t_I \leq DT \leq (t_I + t_{II})$.

C. Mode 3: $t_2 < t < t_3$

In this mode, S_1 and S_4 are conducting and i_p changes linearly with same slope as in the previous mode. Equivalent circuit during this mode is shown in Figure 3b. The primary current $i_p(t)$ is given as $i_p(t) = \frac{V_{dc}}{L}(t - t_2)$. In secondary, the current is transferred linearly from D_6, D_7 to D_5, D_8. This mode ends at t_3 when i_p reaches nI_o and D_6 and D_7 are reverse biased. The time interval is given as $t_{III} = t_3 - t_2 = \frac{nLI_o}{V_{dc}}$.

D. Mode 4: $t_3 < t < t_4$

As D_5, D_8 are conducting, the capacitances across reverse biased diodes D_6, D_7 are in parallel with the series combination of C and C_{snb} (see Fig. 1). As $C \gg C_{snb}$, $\frac{CC_{snb}}{C+C_{snb}} \simeq C_{snb}$. Hence the effective capacitance seen from primary is $C_S = n^2(2C_D + C_{snb})$. The transformer leakage inductance (L) and C_S form a resonating circuit as shown in Figure 4a. The initial values of i_p and v_l' are $i_p(t_3) = nI_o$ and



(a) (b)

Fig. 4. Equivalent Circuits in (a) Mode 4, (b) Mode 5

$v_l'(t_3) = 0$. where v_l' is the rectifier output voltage referred to primary and $nv_l' = v_l$. $i_p(t)$ and $v_l'(t)$ are given as

$$\begin{aligned} i_p(t) &= nI_o + \frac{V_{dc}}{\sqrt{L/C_S}} \sin\big(\omega_2(t - t_3)\big) \\ v_l'(t) &= V_{dc}\big[1 - \cos\big(\omega_2(t - t_3)\big)\big] \end{aligned} \tag{3}$$

where $\omega_2 = \frac{1}{\sqrt{LC_S}}$. At $t = t_4'$, v_l reaches nV_{dc}. The duration $t_4' - t_3 = \frac{\pi\sqrt{LC_S}}{2}$. This mode ends at $t = t_4$ when v_l reaches V_C and D_{snb} is forward biased. Solving (3), the duration of Mode 4 is given as $t_{IV} = t_4 - t_3 = \sqrt{LC_S}\cos^{-1}\left(1 - \frac{V_C}{nV_{dc}}\right)$. And i_p at the end of this mode is given as $i_p(t_4) = nI_o + \sqrt{\frac{V_C}{n}\left(2V_{dc} - \frac{V_C}{n}\right)\frac{C_S}{L}}$. Due to the active snubber $V_C \simeq V_{dc}$. Hence t_{IV} can be approximated as $\frac{\pi\sqrt{LC_S}}{2}$.

E. Mode 5: $t_4 < t < t_5$

In this mode the active clamp circuit is in operation as D_{snb} is forward biased. v_l is clamped to V_C. Equivalent circuit during this mode is shown in Fig. 4b. In this duration i_p and v_l' are given as

$$\begin{aligned} i_p(t) &= i_p(t_4) - \frac{V_C/n - V_{dc}}{L}(t - t_4) \\ v_l'(t) &= V_C/n \end{aligned} \tag{4}$$

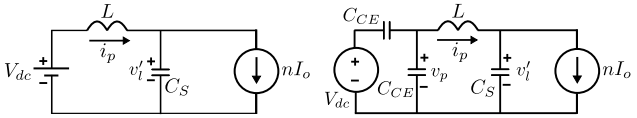
i_p falls linearly. This mode ends at $t = t_5$ when $i_p(t)$ reaches nI_o and current through D_{snb} becomes zero. Using (4), the time interval t_V is given as

$$t_V = t_5 - t_4 = \frac{\sqrt{V_C(2nV_{dc} - V_C)}}{V_C - nV_{dc}}\sqrt{LC_S} \tag{5}$$

As the active snubber is used to reduce the voltage stress, it is desired to operate V_C close to nV_{dc}. Hence $(V_C - nV_{dc})^2 << (nV_{dc})^2$. So (5) can be approximated as $t_V \approx \frac{nV_{dc}\sqrt{LC_S}}{V_C - nV_{dc}}$.

F. Mode 6: $t_5 < t < t_6$

This is an active power transfer mode. Equivalent circuit during this mode is shown in Fig. 5a. In this mode i_p and v_l'



(a) (b)

Fig. 5. Equivalent Circuits in (a) Mode 6, (b) Mode 7

can be expressed as

$$\begin{aligned} i_p(t) &= nI_o - \frac{(V_C/n - V_{dc})}{\sqrt{L/C_S}} \sin\big(\omega_2(t - t_5)\big) \\ v_l'(t) &= V_{dc} + (V_C/n - V_{dc}) \cos\big(\omega_2(t - t_5)\big) \end{aligned} \tag{6}$$

Here power transfer happens with the DC components nI_o and V_{dc}. The link voltage, $v_l(t) = nv_l'(t)$ oscillates around nV_{dc} with an amplitude of $V_C - nV_{dc}$. Due to lossy elements of the practical circuit, the oscillation dies down and v_l and i_p settle to nV_{dC} and nI_o respectively. This mode ends at t_6 when S_4 is turned OFF. The duration, t_{VI} is given as- $t_{VI} = (t_6 - t_5) = dT_s/2 - t_I - t_{II} - t_{III} - t_{IV} - t_V$ where $\frac{dT_s}{2}$ is the duration of active power transfer (see Fig. 2a) and d is the duty ratio. Here it is defined as the time between turn OFF of S_2 to turn OFF of S_4.

G. Mode 7: $t_6 < t < t_7$

After S_4 is turned OFF at $t = t_6$, the voltage across it cannot change immediately due to switch capacitance C_{CE}. Channel current through the device falls before any change in device drain to source voltage which results in ZVS turn OFF of S_4. Equivalent circuit in this mode is shown in Fig. 5b. The

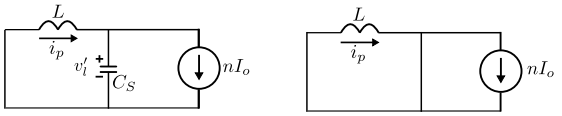
voltage across the devices are $v_{S_3} = v_p$ and $v_{S_4} = V_{dc} - v_p$. In this mode $i_p(t)$, $v_p(t)$ and $v_l'(t)$ are given as

$$\begin{aligned} i_p(t) &= \frac{nI_o}{C_P + C_S}\left[C_P + C_S\cos\left(\omega_3(t-t_6)\right)\right] \\ v_p(t) &= V_{dc} - \frac{nI_o}{(C_P+C_S)}\left[(t-t_6) + \frac{1}{\omega_3}\left(\frac{C_S}{C_P}\right)\sin\left(\omega_3(t-t_6)\right)\right] \\ v_l'(t) &= V_{dc} - \frac{nI_o}{C_P+C_S}\left[(t-t_6) - \frac{1}{\omega_3}\sin\left(\omega_3(t-t_6)\right)\right] \end{aligned} \tag{7}$$

where $\omega_3 = \frac{1}{\sqrt{L(C_PC_S/(C_P+C_S))}}$. Third order dynamics are observed in the expressions of v_p and v_l'. This mode ends at $t = t_7$ when v_p reaches 0 and D_3 is forward biased. It is observed that with large leakage and at rated load, the fast dynamics of C_P and L leads to a shorter interval of mode 7 i.e $\omega_3(t_7 - t_6) << 1$, which leads to following approximations- $i_p(t) \approx nI_o$, $v_p(t) \approx V_{dc} - \frac{nI_o}{C_P}(t-t_6)$, $v_l'(t) \approx V_{dc}$ and $t_{VII} = t_7 - t_6 \approx \frac{V_{dc}C_P}{nI_o}$. The condition for this approximation is given as $\left(\frac{V_{dc}}{nI_o}\sqrt{\frac{C_P}{L}}\sqrt{1+\frac{C_P}{C_S}}\right) \ll 1$. This actually implies that i_p and v_l' remain constant and v_p falls linearly (as known in existing literature).

H. Mode 8: $t_7 < t < t_8$

In this mode S_1 and the anti-parallel diode of S_3 are conducting and thus shorting the primary winding of the transformer. Equivalent circuit in this mode is shown in Fig. 6a. The gating signal of S_3 can be applied now to ensure ZVS turn ON. Hence, the minimum required dead time (DT) of $S_3 - S_4$ is given as $DT \geq t_{VII}$. i_p and v_l' are given as



(a) (b)

Fig. 6. Equivalent Circuits in (a) Mode 8, (b) Mode 9

$$\begin{aligned} i_p(t) &\approx nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}\sin\left(\omega_2(t-t_7)\right) \\ v_l'(t) &\approx V_{dc}\cos\left(\omega_2(t-t_7)\right) \end{aligned} \tag{8}$$

The link voltage $v_l(t) = nv_l'(t)$. This mode ends at $t = t_8$ when v_l' reaches zero and D_6, D_7 are forward biased. The time interval t_{VIII} is estimated solving (8).

$$\begin{aligned} t_{VIII} &= t_8 - t_7 = \frac{\pi\sqrt{LC_S}}{2} \\ i_p(t_8) &\approx nI_o - \frac{V_{dc}}{\sqrt{L/C_S}} \end{aligned} \tag{9}$$

Due to periodic nature of the waveform with half-wave symmetry, the magnitude of i_p derived in this mode is used as initial condition in Mode 1.

I. Mode 9: $t > t_8$

In this mode, both v_p and v_l are clamped to zero. The converter is in free-wheeling state. Equivalent circuit in this mode is shown in Fig. 6b. The primary current is given as $i_p(t) = nI_o - \frac{V_{dc}}{\sqrt{L/C_S}}$. All four diodes of secondary rectifier are conducting. To achieve ZVS turn ON of S_3, gating pulse is applied in this mode. The mode ends when S_1 is turned OFF and the circuit enters into a similar mode as Mode 1. The duration of the mode is given as in (10).

$$t_{IX} = \frac{(1-d)T_s}{2} - t_{VII} - t_{VIII} \tag{10}$$

In the next half of the flux balance cycle (T_s) the circuit evolves through similar modes as discussed above.

III. Computation of Output voltage

$$\begin{aligned} V_o =& \frac{2}{T_s}\int_0^{T_s/2} v_l(t)dt \\ =& \frac{2}{T_s}\left[\int_{t_3}^{t_4} nV_{dc}\left[1-\cos\left(\omega_2(t-t_3)\right)\right]dt + V_Ct_V \right. \\ & \left. + nV_{dc}(t_{VI}+t_{VII}) + \int_{t_7}^{t_8} nV_{dc}\cos\left(\omega_2(t-t_7)\right)dt\right] \\ =& \frac{2}{T_s}\left[nV_{dc}t_{IV} + V_Ct_V + nV_{dc}(t_{VI}+t_{VII})\right] \\ =& \frac{2}{T_s}\left[nV_{dc}t_{IV} + (V_C - nV_{dc})t_V + nV_{dc}(t_V + t_{VI} + t_{VII})\right] \\ =& dnV_{dc} - \frac{4n^2LI_o}{T_s} + \frac{2nV_{dc}}{\pi}\frac{\omega_s}{\omega_2} = \boxed{nV_{dc}\left(d + \frac{2}{\pi}\frac{\omega_s}{\omega_2}\right) - R_oI_o} \end{aligned} \tag{11}$$

Considering ideal operation of the converter, the output voltage is $V_o = ndV_{dc}$. But the profile of the link voltage v_l and duration of active states are changed due to parasitics and active snubber clamp (see Fig. 2b). Considering all non idealities, a closed form expression of V_o is presented here. The average output voltage can be given as in (11), where $\omega_s = \frac{2\pi}{T_s}$ and $R_o = 4n^2L/T_s$. In the above derivation we have considered $t_I \approx t_{VII}$ and $t_{IV} \approx t_{VIII}$. The expressions of the time intervals of different modes derived in the last section are used here. As seen in (11), in the expression of V_o there is an increase in duty cycle, $\frac{2\omega_s}{\pi\omega_2}$ along with the well-known duty-cycle loss due to leakage inductance. When ω_2 is comparable with ω_s, the effect of secondary capacitance (duty cycle increase) can not be ignored. Another important observation is that the expression of V_o is independent of active snubber clamp voltage V_C.

IV. Estimation of parasitics

To estimate the output voltage (V_o), the values of parasitics, L and C_s are required (see (11)). What follows is a method of estimation of these parasitics from experimental waveforms.

A. Estimation of L

From the experimental waveform of i_p, the current slope (K_1) can be evaluated in Mode 2 and 3. Then L can be given as $L = \frac{V_{dc}}{K_1}$. Again, in Mode 5, the slope of i_p is estimated as K_2. L is given as $L = \frac{V_C/n - V_{dc}}{K_2}$.

B. Estimation of C_s

From the experimental waveform of v_l, the period of oscillation T_{osc} can be estimated in Mode 6. The effective capacitance $C_S = \left(\frac{T_{osc}}{2\pi}\right)^2 \frac{1}{L}$. It can also be estimated from the duration of Mode 4 as follows $C_s = \frac{t_{IV}^2}{L\left(\cos^{-1}\left[1 - \frac{V_C}{nV_{dc}}\right]\right)^2}$.

V. Experimental Verification

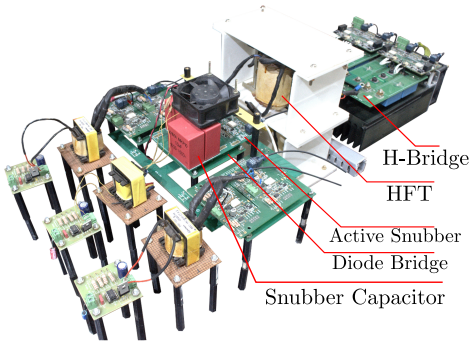


Fig. 7. Hardware prototype

A PSFB is designed to experimentally validate the converter operation. The specifications of the prototype are listed in Table I. The setup is shown in Fig. 7. The primary bridge is implemented with Semikron IGBT modules SKM50GB12T4. The secondary rectifier is implemented with 3kV SiC Schottky diodes GAP3SLT33-214. EPCOS ferrite E cores E80/38/20 are used for the high frequency transformer. The key experimental waveforms of v_p, v_l and i_p are shown in Fig. 8. In the figure, the modes of operation and durations are marked. The experimental result closely matches with the analytical waveforms shown in Fig. 2b. Observed clamp voltage V_C is 1870V. The parasitics L and C_S are estimated following the procedure stated in the last section from the experimental waveform and are tabulated in Table II. The estimated values are $L = 141.6\mu H$ and $C_S = 4.56nF$. For the given operating condition in Table I and measured values of parasitics, using (11) the output voltage (V_o) is analytically estimated as 1244.9V. The actual measured output voltage is 1240V (see Table III). The error in analytical estimation is 0.4%. Fig. 9 shows the ZVS turn ON of S_2 and S_3 respectively. From the figures it is seen that, the gate voltages (G_2 and G_3) rise above threshold when the voltage across the devices (v_{S_2} and v_{S_3}) becomes zero. This confirms the ZVS turn ON as discussed in Mode 2.

TABLE I
Specifications of the Setup

Parameter	Value
Input Voltage (V_{dc})	400 V
Duty (d)	0.85
Turns Ratio (n)	4
Switching Frequency (f_s)	20 kHz
Load current (I_o)	1.2 A
Output Power (P)	1.5kW
Clamp voltage (V_C)	1870V

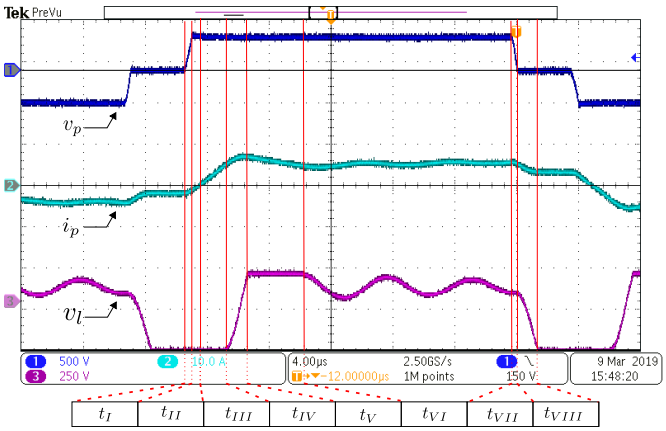


Fig. 8. Experimental waveforms of the converter

TABLE II
Estimation of Parasitics

Parameter	Method of estimation or measurement	value
L	Mode 2 (K_1=2840909 A/s)	140.8 μH
	Mode 5 (K_2=468720 A/s)	142.4 μH
C_S	Mode 6 (T_{osc}=5.03 μs)	4.56 nF
	Mode 4 (t_{IV}=1.4 μs)	4.57 nF

VI. Conclusion

The steady state operation of the phase shifted full bridge converter is analysed considering device and diode output capacitances and transformer leakage inductance. A commonly employed single-switch active clamp is considered to limit the voltage stress of the rectifier diodes. It is observed that the rectifier output of a PSFB deviates significantly from ideal waveform due to dominant effects of the parasitics. Due to

TABLE III
Estimated and Observed Output Voltage (V_o)

Analytically estimated using (11)				Experimentally measured
ndV_{dc}	$2nV_{dc}\omega_s/(\pi\omega_2)$	R_oI_o	V_o	
1360V	102.4V	217.5V	1244.9V	1240V

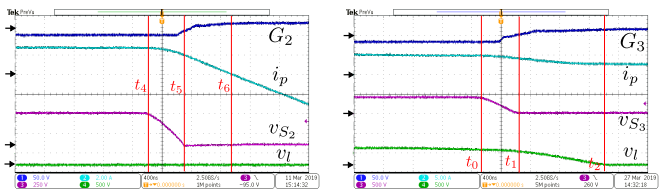


Fig. 9. ZVS turn ON of S_2 and S_3

secondary diode parasitic capacitances, the circulating current during zero state is lower than the reflected load current leading to reduction in ZVS range. The analysis provides an expression for this current which will help in dead-time design to achieve ZVS. A closed form expression of the output voltage is analytically derived and experimentally verified. It is observed that other than the known duty cycle loss due to leakage inductance, there is a duty cycle gain in output voltage due to secondary diode capacitances. These effects of the secondary diode capacitance are generally ignored in the existing analysis of PSFB. It is observed that the output voltage is independent of the snubber clamp voltage. A laboratory prototype of 1.5kW, 400V to 1.25kV PSFB is built. The mode by mode converter operation is experimentally verified. The analytical waveforms are closely matched with the experimental results and clearly show the effects of parasitics on the PSFB operation. The paper also presents an estimation technique to find the values of key parasitics. Presented analysis and estimation technique will be valuable in proper design and control of this widely used isolated DC-DC converter.

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